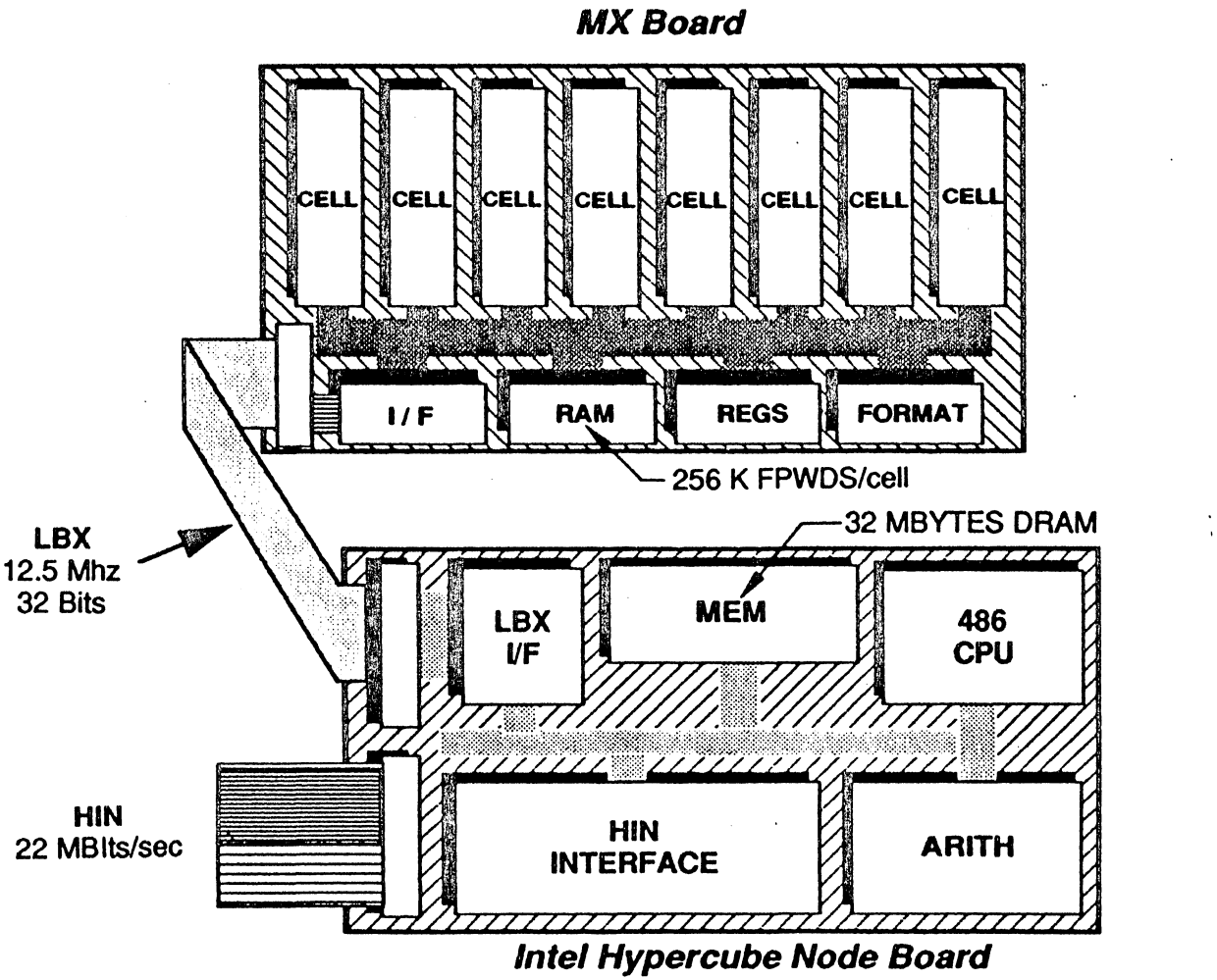
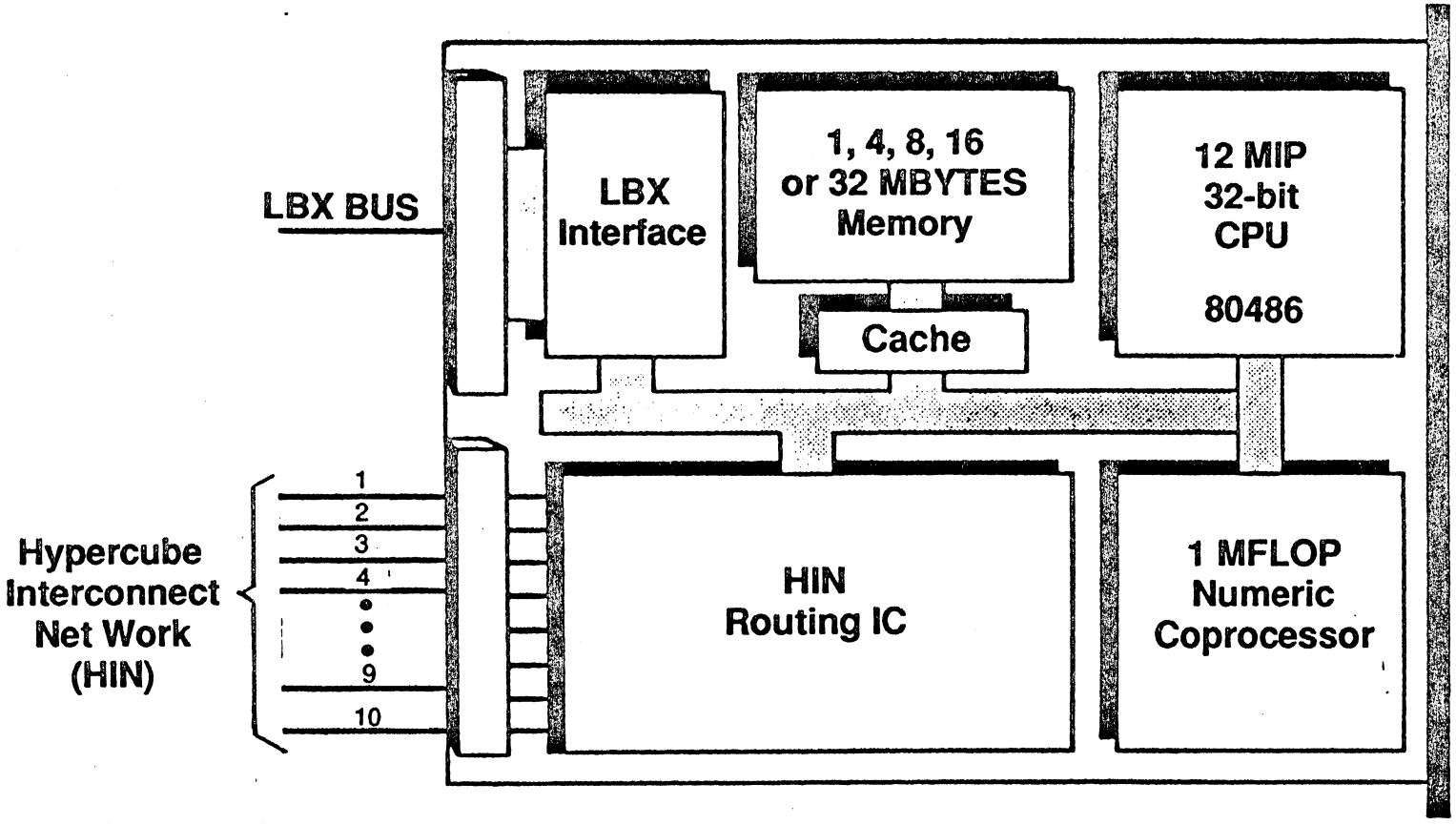
Accelerated Hypercube Computer System

Accelerator Modules With Militarized Hypercube Commercial Computer Provide GFLOPS of Throughput

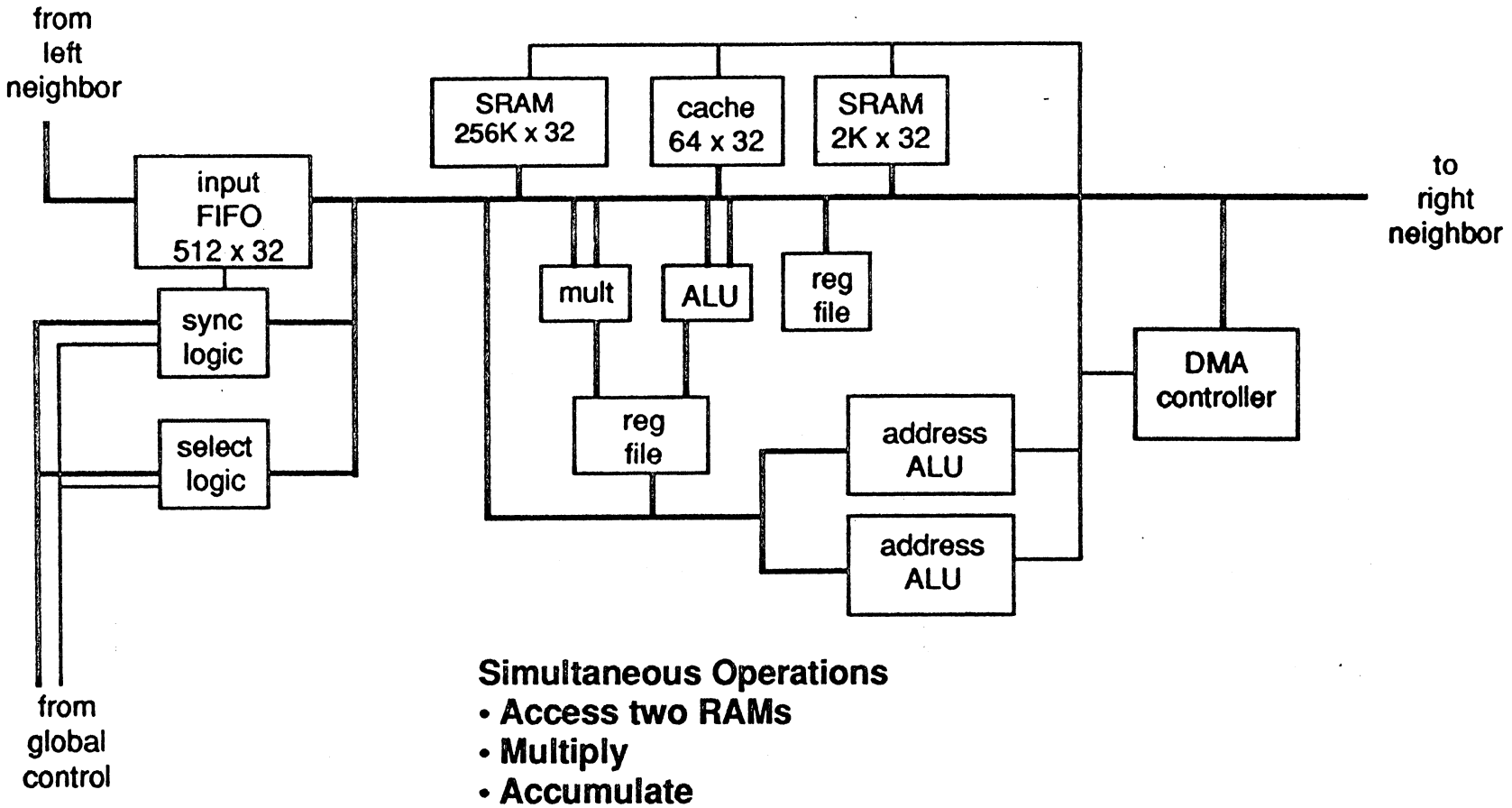


Node Processor Provides 12 MIPS With 32 MBYTES Memory



- HIN is 22 MBITS per second (BIT serial)

Cell Architecture



Simultaneous Operations

- **Access two RAMs**
- **Multiply**
- **Accumulate**
- **Compute two addresses**
- **Fetch next instruction**
- **Input to FIFO**
- **16.5 mHz clock (instructions)**

MX Unique Attributes

132 MFLOPS* on one circuit card

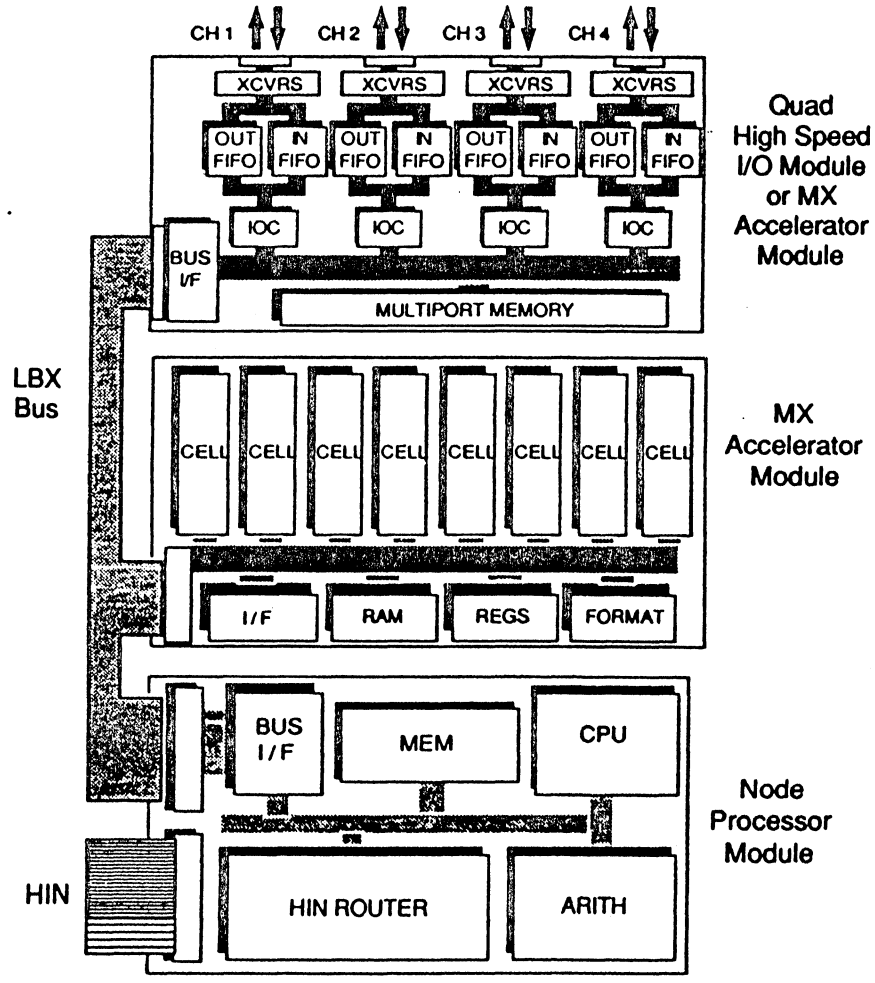
- Allows high-throughput problem to fit on one card
- Eases the partitioning problem

Eight processing elements on one circuit card

- Systolic operation useful in some applications
- MIMD operation useful in other applications

*MFLOP = million floating-point multiply and adds per second

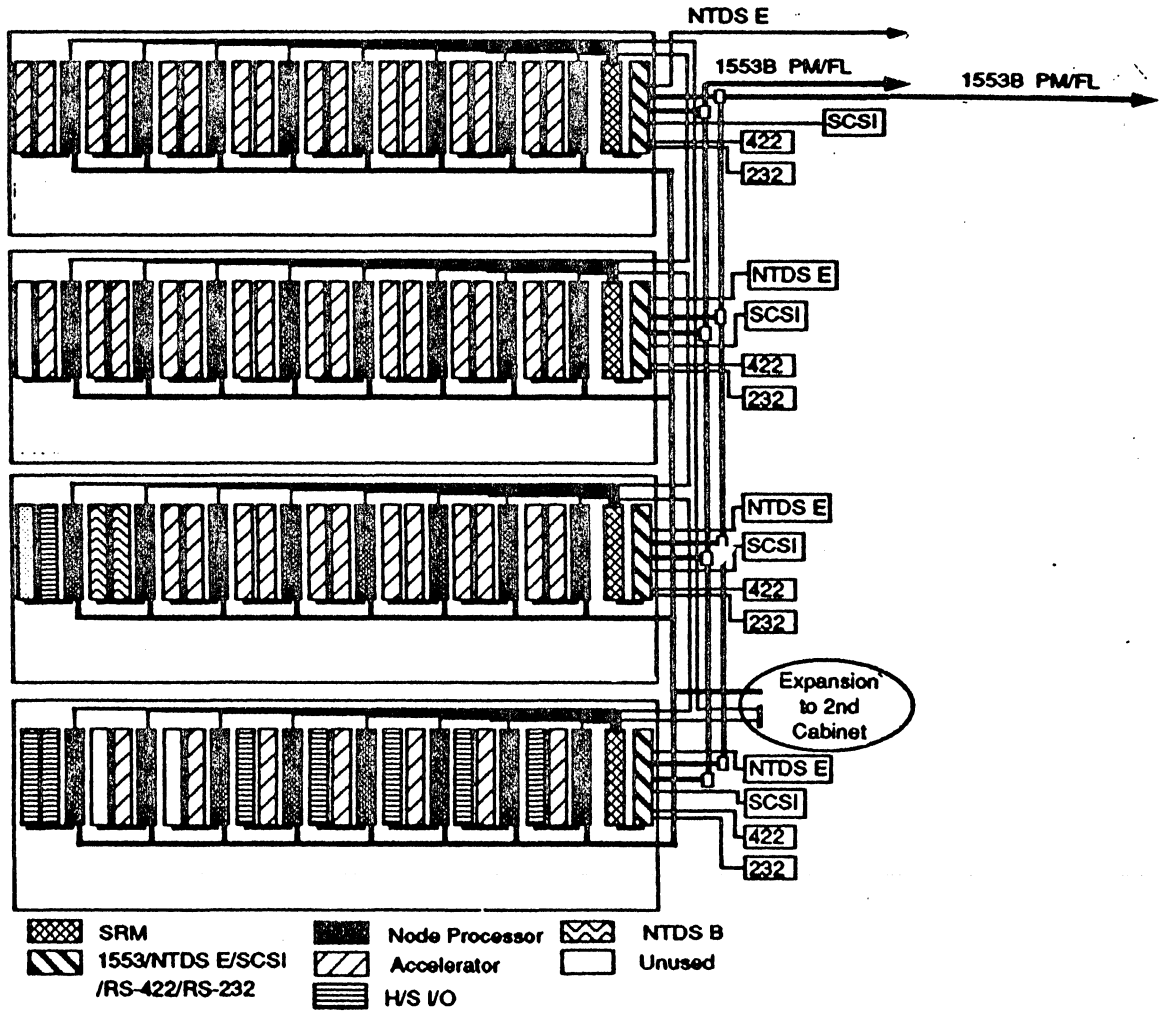
Node Group of Three Modules



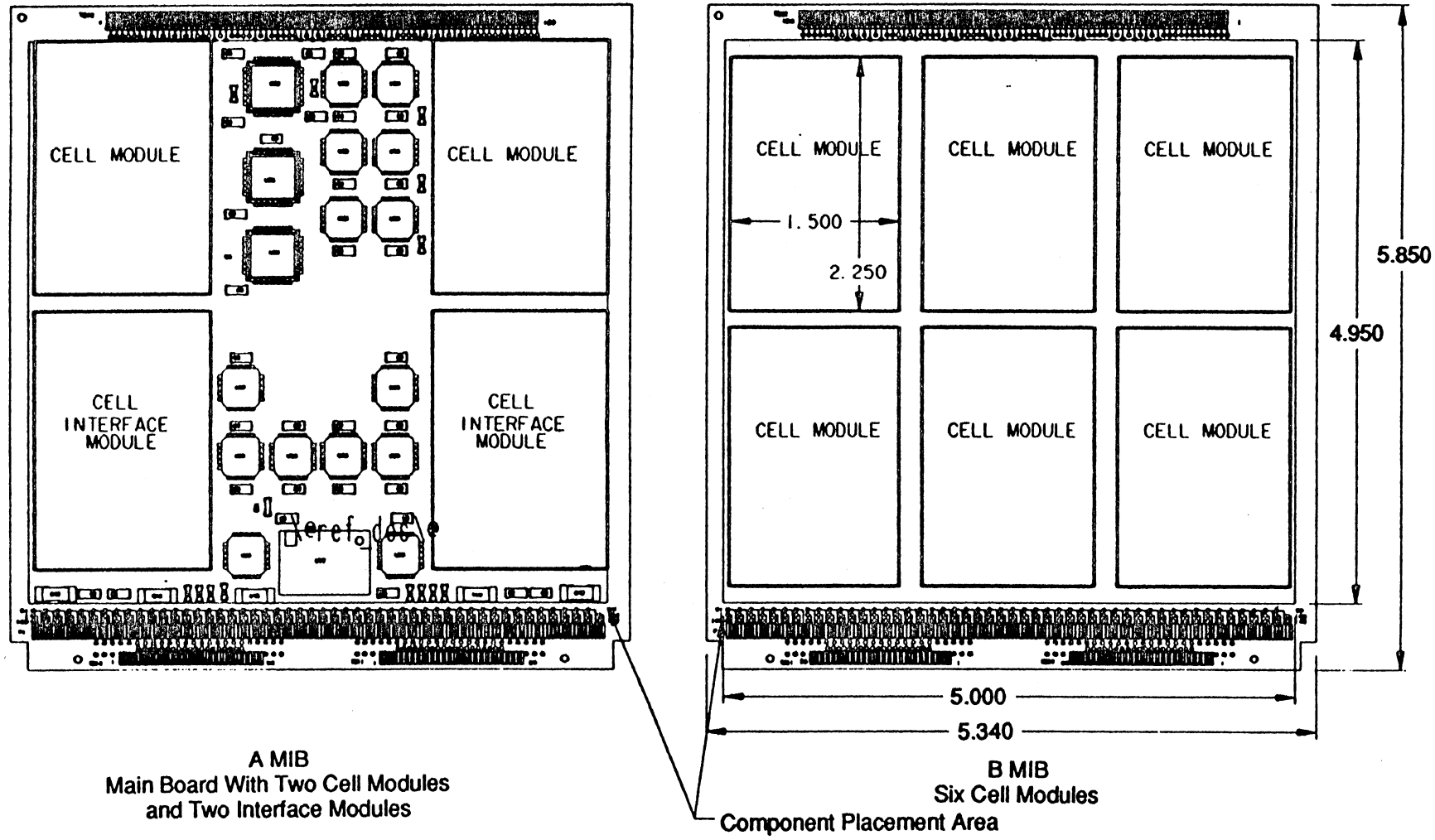
- I/O Channel is 10 MBYTES/sec; half duplex
- IOC is INTEL 80860

A 32-Node Hypercube in One Cabinet Provides 7.4 GFLOPS of Processing, Complex Interconnectivity and 320 MBYTES I/O

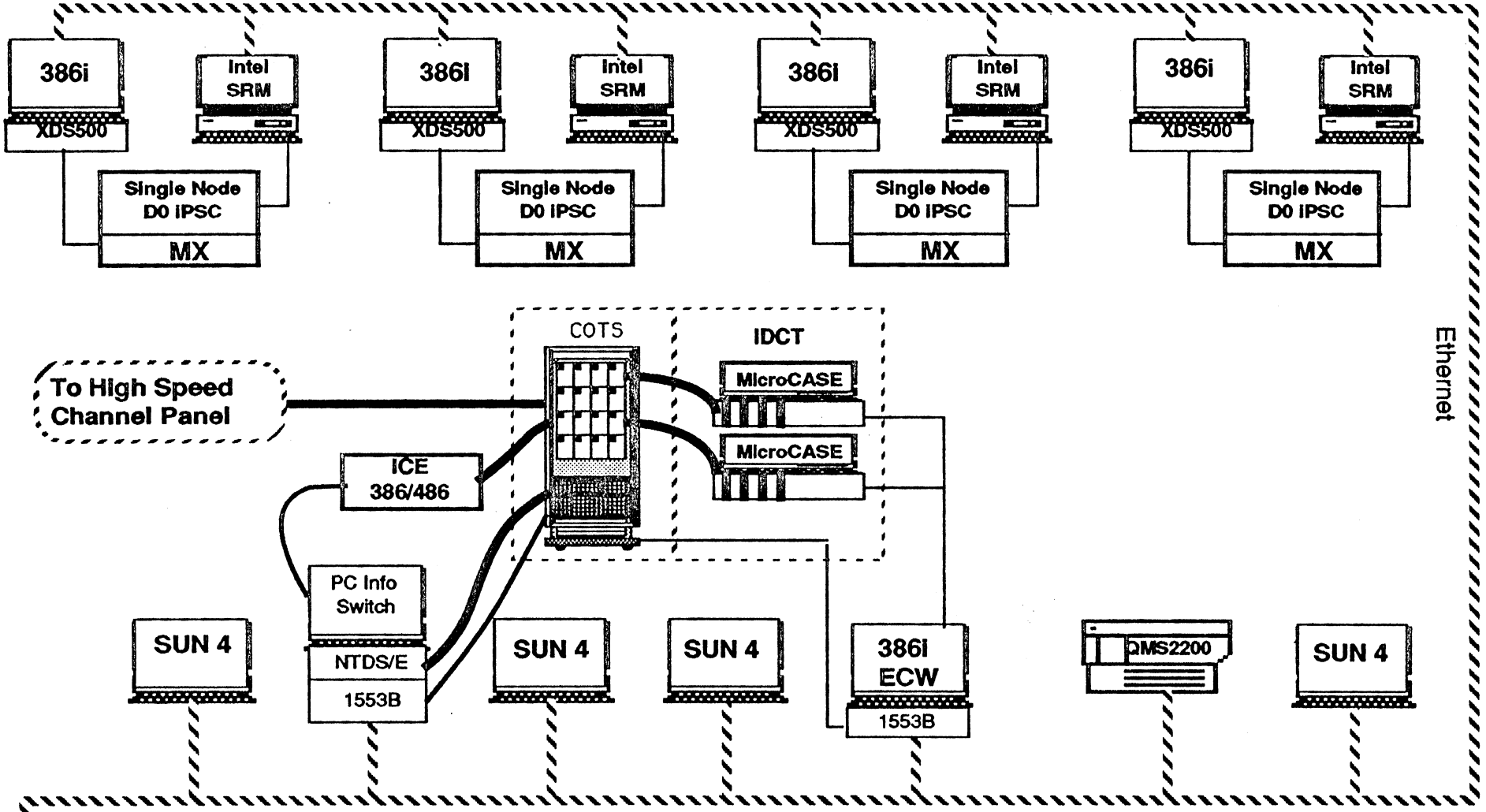
A 32 NODE HYPERCUBE IN ONE CABINET PROVIDES 7.4 GFLOPS OF PROCESSING COMPLEX INTERCONNECTIVITY AND 320 MBYTES I/O



Accelerator SEM E Configuration Using Multichip Cell Modules



CSCI Development Workstations



To Facility Core
(AMIS,CCC,Basis,CRYPTO,
Sherpa & CSDS-I)

Teamwork, ADAS, ACT, EXCEL, WordPerfect, MATLAB
Tartan Lab's TMS320C30 Ada Compiler
Verdix Distributed Ada